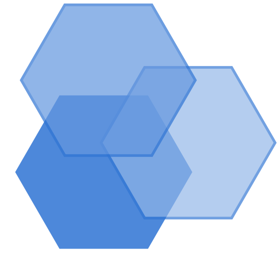
MEASURING HEAT FLUX FROM A COMPONENT ON A PCB



INTRODUCTION

Electronic circuit boards consist of components which generates substantial amounts of heat during their operation. A clear knowledge of the level of heat dissipation from electronic components during their operation is desirable for reliable and optimal design of cooling systems and selection of the appropriate heat removal methodologies, as heat dissipation from a component in an electronic package not only influences its own performance but also affects the performance of neighboring components, leading to their failure.

Progressively, the demand for higher power density and efficiency in electronic products is increasing. This leads to a greater need for accurate means of measuring the dissipative losses of power and the knowledge of this heat dissipation from electronic components is a critical input for thermal designers. Conventional techniques for measuring the heat dissipation include the integration of the product of measured voltage and current and the use of insulated calorimetry chambers to measure the heat flow from the devices. Calorimetric methods have been used to make loss measurements of electric machines or standalone components such as power electronic device, transformer, ferrite and capacitor etc.

A method proposed [1] in this article, to measure heat dissipation of components on a printed circuit board (PCB) under operating conditions, utilizes a heat flux sensor and themistors, and calculates heat dissipation from a thermal standpoint. Measurement is prone to error due to interference of the neighboring component (heat sources) and this is compensated by carrying out error analysis, with the help of which an Error Indicator is developed. In order to validate and prove the effectiveness of this new method, experiments are carried out and exhibited a close match between the measured and experimental values.

MEASUREMENT METHOD

Consider a 2-node thermal resistance network as shown in figure 1 below

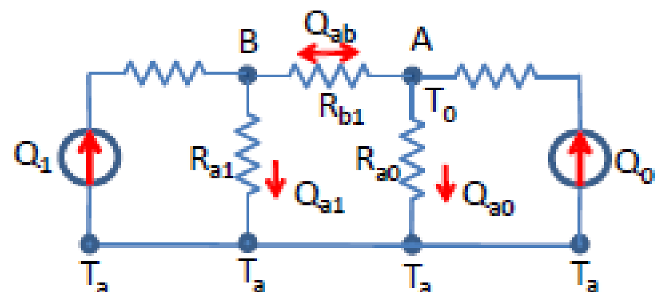


Figure 1. 2-Node Thermal Resistance Network [1]

There are 2 nodes, A and B that are heat sources. Nodes A and B are connected to each other and to the ambient sink.

Node A details:

- Heat dissipation: Q_0
- Temperature: T_0
- Heat dissipation from node A to sink: Q_{a0}

Node B details:

- Heat dissipation: Q_1
- Heat dissipation from node B to sink: Q_{a1}

Also, T_a represents ambient temperature and Q_{ab} is the heat exchange between nodes A and B.

For this network, heat dissipation from node A to sink is given in equation 1. The temperature difference between temperature at node A and ambient temperature is basically a combination of heat dissipation at node A and some heat from node B and is given in equation 2 below. Equation 3 shows that the resistance $1/R_1$ is proportional to resistances only.

$$Q_{a0} = \frac{R_{a1}}{R_{a0} + R_{b1} + R_{a1}} \cdot Q_1 + \frac{R_{b1} + R_{a1}}{R_{a0} + R_{b1} + R_{a1}} \cdot Q_0 \qquad (1)$$

$$Q_0 + \frac{R_{a1}}{R_{b1} + R_{a1}} \cdot Q_1 = \frac{1}{R_1} \cdot (T_0 - T_a) \qquad (2)$$

$$\frac{1}{R_1} = \frac{1}{R_{a0}} + \frac{1}{R_{b1} + R_{a1}} \qquad (3)$$

Thermal resistance network shown in figure 2 below depicts different components on PCB. Nodes labeled as A, B, C, D and E are dissipating heat while other nodes shown do not dissipates heat. Node A is the Device Under Test (DUT) whose heat dissipation is measured by this method.

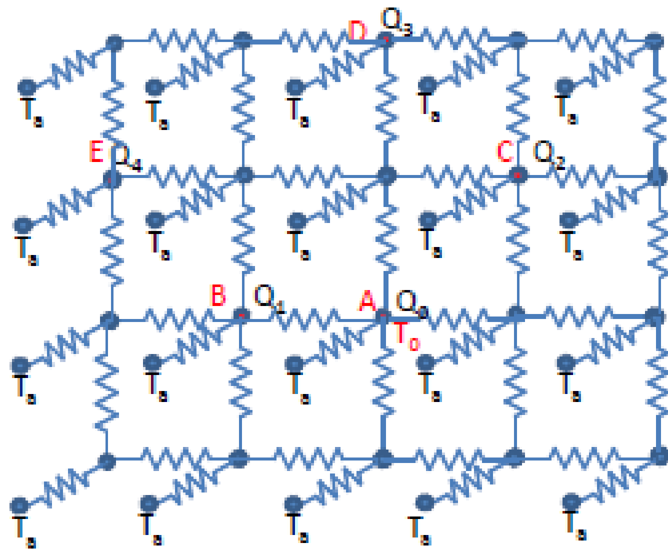


Figure 2. Thermal Resistance Network for the General Case [1]

As explained in the previous section, $(T_0 - T_a)$ is basically proportional to the heat dissipation at node A and combination of heat dissipation from other nodes in the network, like from node B, C, D, E and is given by:

$$Q + E = Q_m + K \cdot (T_0 - T_a) \qquad (4)$$

Please note that this technique is ignoring all radiation heat transfer gain and loss. The above equation has two unknowns and two measurable parameters. K is an unknown constant and is the reciprocal of thermal resistance from T_0 to T_a. Q+E is another unknown constant. Q is the total heat dissipation from DUT and E is the effect of other heat sources on the PCB. Q_m in the equation is basically a measured quantity. It is part of total heat dissipation Q which is drawn away through components case top and not through the network. This is done and measured using thermoelectric module, which draw different amounts of heat from the component case top and monitors the change in Q_m. As Q_m changes, T_0-T_a also changes and is also monitored. Figure 3 shows the result of calculation based on equations 1-3 where Q+E is the predicted heat dissipation for the DUT. Of this, Q is the actual heat dissipation and E is artificial part. Equation 4 has two unknowns K and Q+E. Q_m can be varied using a TEC which results in different T_0-T_a. By taking two sets of data Q+E can be calculated.

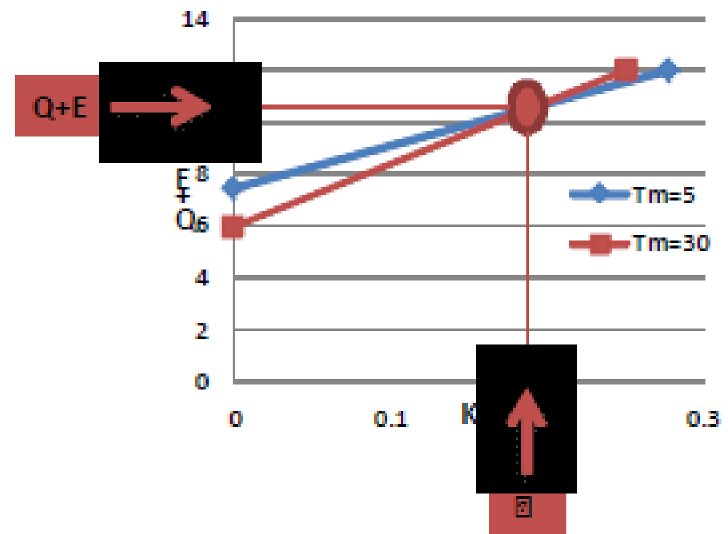


Figure 3. Calculation Graph [1]

TEST METHOD

Heat flux sensor, Thermoelectric cooling module (TEC), thermistor are used in testing the entire PCB assembly which is placed in a wind tunnel with high cooling air flow rate. The arrangement is as shown in figure 4 wherein, heat flux sensor is placed between the DUT and the TEC with active heat sink. A total of five thermistors are used and attached on other side of PCB (side other than where DUT is mounted). One thermistor is attached exactly below the DUT

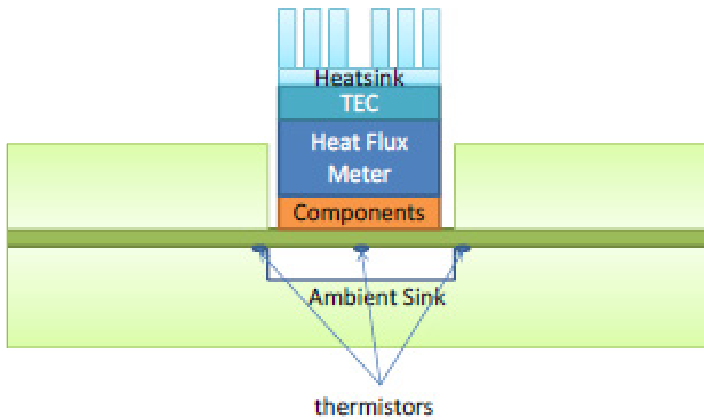


Figure 4. Testing Apparatus [1]

at the centre and four other thermistors are attached at the mid points of the four edges of DUT. TEC used is modulated to draw different amounts of heat from the DUT. The intent is, the heat flow should be maximum from the center and should spread from center to the sides. To achieve this, the average temperature from the four surrounding points of DUT is lower than or equal to that in the middle of DUT.

This testing set up and method is OK if the DUT is the only heat source on the PCB, but does not hold true if there are heat sources other than DUT. In that case, as shown in equation 4, interference from nearby heat sources (E) comes in to picture and should be considered to avoid the obvious error in heat dissipation estimation.

NEED FOR ERROR INDICATOR AND ITS DERIVATION

From equation 2 and equation 4 above, the interference term E is given as

$$E = \frac{R_{a1}}{R_{b1} + R_{a1}} \cdot Q_1 \qquad (5)$$

Looking at the interdependency of the parameters in equation 5, there are three factors that affect the theoretical measurement error and raises the need to derive an Error Indicator:

1. When heat flow from nearby source (Q_1) is smaller, the error becomes smaller
2. When the nearby heat source is far away from DUT or the board in plane conductivity is less, then R_{b1} is larger and the error becomes smaller
3. When there is higher cooling rate near Q_1, R_{a1} is smaller and the error becomes smaller

During testing, only cooling rate can be controlled, whereas other two factors are out of measurement control. In order to compensate the effect of error overall and achieve highly accurate measurement, an Error Indicator is required which can be used during testing and reveal the measurement method error.

A concept of Isotherm Hierarchy is used to define an error indicator. Figure 5 shows a topology of heat transfer from DUT and other n heat sources flowing through a hierarchy of isotherms to ambient sink. Figure 6 shows the isotherms hierarchy on PCB plane and thermal resistance network. Let T_b locates at the center of DUT. Let T_n be the 1st isotherm surrounding the DUT only, T_{n+1} be the 2nd isotherm surrounding the DUT and first closest neighbor heat source, T_{n+2} be the 3rd isotherm surrounding the DUT and the first two closest neighbor heat sources, so on and so forth, till T_{n+n} circles all the n neighbor heat sources. It is not necessary for T_{n+I} to be higher than T_{n+i+1}. Heat flow Q_{bi} (i=1, ..., n) will alter direction to comply with the law of heat flowing from a high temperature node to a lower temperature node. Figure 7 is the equivalent network for all the heat sources and is basically a transformation of figure 6.

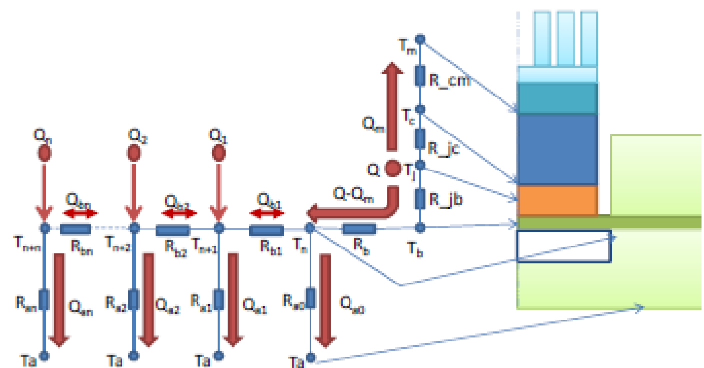


Figure 5. A Topology of Heat Flow to Ambient [1]

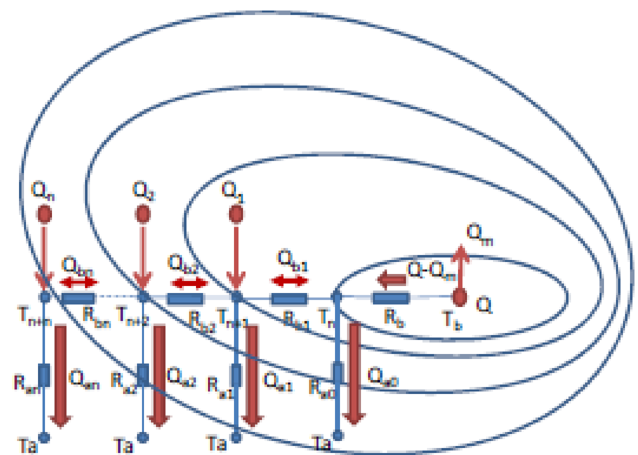


Figure 6. n-Node Thermal Resistance Network [1]

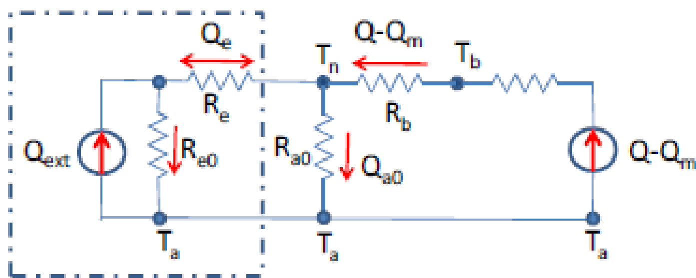


Figure 7. Equivalent Thermal Resistance Network [1]

All the nearby heat sources are replaced with an equivalent heat source Q_{ext}. Rearranging equation 4 and including T_b, we get equation 6 as follows,

$$Q + \frac{\frac{R_{e0}}{R_{e0}+R_e}}{1 + R_b \cdot \left(\frac{1}{R_{a0}} + \frac{1}{R_{a0}+R_e}\right)} \cdot Q_{ext}$$

$$= Q_m + \frac{\left(\frac{1}{R_{a0}} + \frac{1}{R_{e0}+R_e}\right)}{1 + R_b \cdot \left(\frac{1}{R_{a0}} + \frac{1}{R_{e0}+R_e}\right)} \cdot (T_b - T_a) \qquad (6)$$

The error percentage due to neighbor heat sources Q_{ext} is given in equation 7,

$$\text{Error\%} = \frac{\frac{R_{e0}}{R_{e0}+R_e} \cdot Q_{ext}}{1 + R_b \cdot \left(\frac{1}{R_{a0}} + \frac{1}{R_{e0}+R_e}\right) \cdot Q}$$

$$= \frac{R_{a0} \cdot \frac{R_{e0}}{R_{a0}+R_{e0}+R_e} \cdot Q_{ext}}{\left(R_b + R_{a0} \cdot \frac{(R_{e0}+R_e)}{R_{a0}+R_{e0}+R_e}\right)} \qquad (7)$$

When TEC draws all the heat from the component case top, $Q - Q_m$ is close to zero.
Therefore,

$$R_{a0} \cdot \frac{R_{e0}}{R_{a0}+R_{e0}+R_e} \cdot Q_{ext} = T_n - T_a \text{ (when } Q_m = Q) \qquad (8)$$

When TEC draws almost none of the heat through case top, Q is close to $(Q - Q_m)$. Equation 9 therefore is:

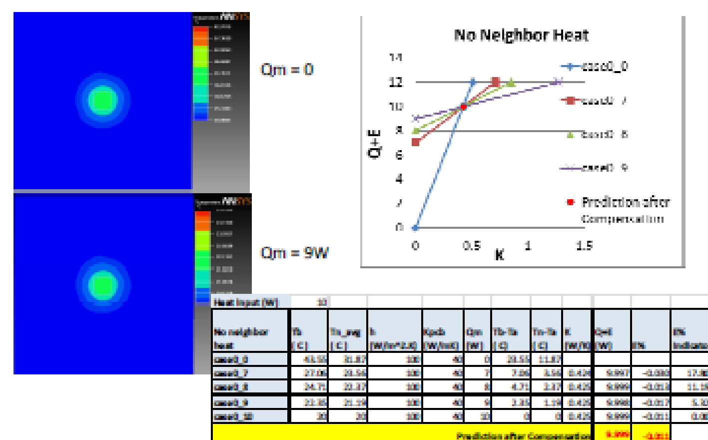
$$\left(R_b + R_{a0} \cdot \frac{(R_{e0}+R_e)}{R_{a0}+R_{e0}+R_e}\right) \cdot Q$$

$$= (T_b - T_a)(\text{when} Q_m = 0) - (T_n - T_a)(\text{when} Q_m = 0) \qquad (9)$$

The error percentage calculated using the above equations and applying them to experimental set up, is the measurement method error due to the nearby heat sources interference.

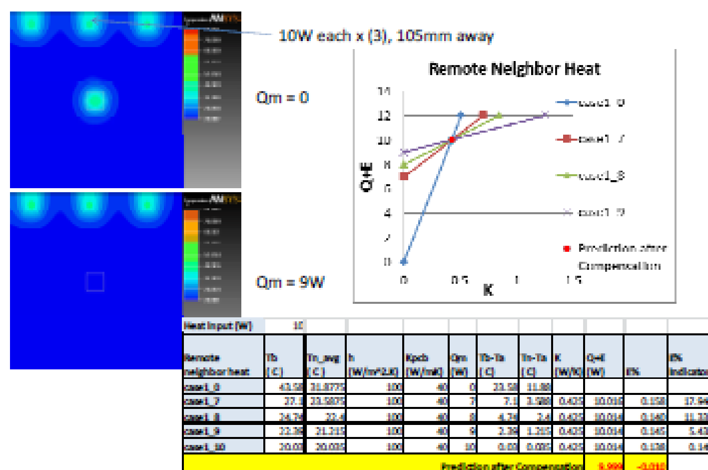
Comparison between Simulations and Measurement using Error Indicator

Ten cases of different power levels and different distance of sources from the DUT, varying PCB conductivities and ambient cooling rates are simulated with ANSYS Icepak. Figures 8, 9, 10, 11 show four simulated cases results with different nearby heat sources on PCB.



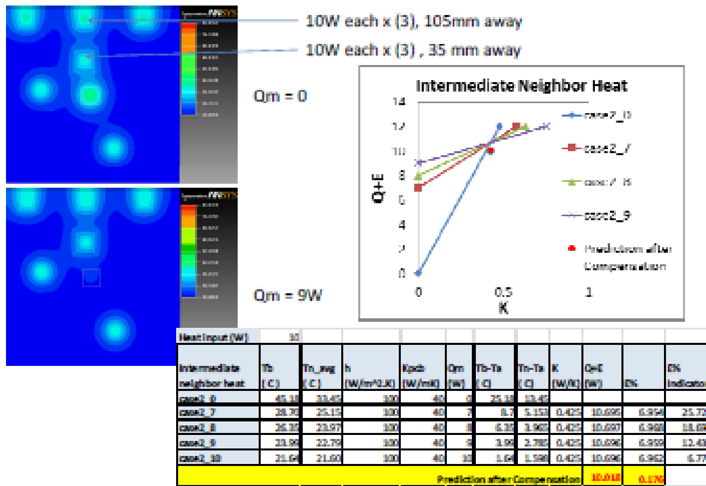
Heat Input (W)	10										
No neighbor heat	Tb [C]	Tn_avg [C]	h [W/m^2.K]	Kpcb [W/mK]	Qm [W]	Tb-Ta [C]	Tn-Ta [C]	K [W/K]	Q+E [W]	E%	E% Indicator
case0_0	43.55	31.87	100	40	0	23.55	11.87				
case0_7	27.06	23.56	100	40	7	7.06	3.56	0.428	9.997	-0.030	17.809
case0_8	24.71	22.37	100	40	8	4.71	2.37	0.425	9.999	-0.013	11.190
case0_9	23.35	21.19	100	40	9	3.35	1.19	0.425	9.998	-0.017	5.322
case0_10	20	20	100	40	10	0	0	0.425	9.999	-0.011	0.000
Prediction after Compensation									9.999	-0.011	

Figure 8. Case 0 – No Neighbor Heat Source [1]



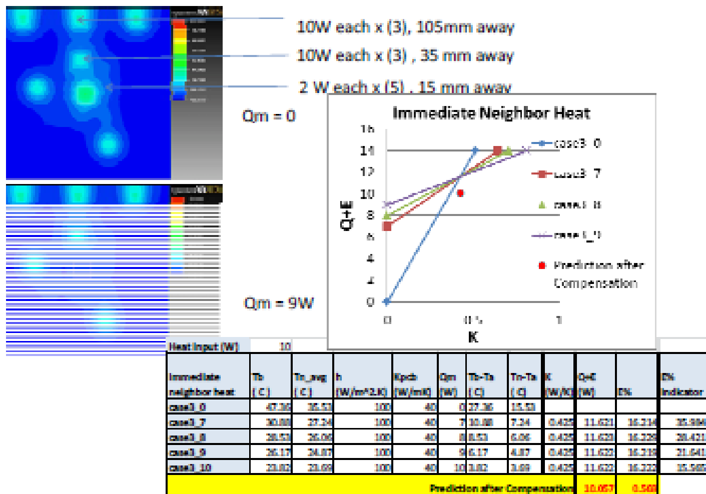
Heat Input (W)	10										
Remote neighbor heat	Tb [C]	Tn_avg [C]	h [W/m^2.K]	Kpcb [W/mK]	Qm [W]	Tb-Ta [C]	Tn-Ta [C]	K [W/K]	Q+E [W]	E%	E% Indicator
case1_0	43.58	31.8775	100	40	0	23.58	11.88				
case1_7	27.1	23.5875	100	40	7	7.1	3.588	0.425	10.016	0.158	17.944
case1_8	24.74	22.4	100	40	8	4.74	2.4	0.425	10.014	0.140	11.331
case1_9	22.39	21.215	100	40	9	2.39	1.215	0.425	10.014	0.145	5.433
case1_10	20.03	20.035	100	40	10	0.03	0.035	0.425	10.014	0.138	0.146
Prediction after Compensation									9.999	-0.010	

Figure 9. Case 1 – Remote Neighbor Heat Sources [1]



Heat Input (W)	10										
Intermediate neighbor heat	Tb (C)	Tn_avg (C)	h (W/m^2.K)	Kpcb (W/mK)	Qm (W)	Tb-Ta (C)	Tn-Ta (C)	K (W/K)	Q+E (W)	E%	E% Indicator
case2_0	45.18	33.45	100	40	0	25.18	13.45				
case2_7	28.70	25.15	100	40	7	8.7	5.153	0.425	10.695	6.954	25.727
case2_8	26.35	23.97	100	40	8	6.35	3.965	0.425	10.697	6.968	18.690
case2_9	23.99	22.79	100	40	9	3.99	2.785	0.425	10.696	6.959	12.436
case2_10	21.64	21.60	100	40	10	1.64	1.598	0.425	10.696	6.962	6.774
								Prediction after Compensation	10.018	0.176	

Figure 10. Case 2 – Intermediate Neighbor Heat Sources [1]



Heat Input (W)	10										
Immediate neighbor heat	Tb (C)	Tn_avg (C)	h (W/m^2.K)	Kpcb (W/mK)	Qm (W)	Tb-Ta (C)	Tn-Ta (C)	K (W/K)	Q+E (W)	E%	E% Indicator
case3_0	47.36	35.53	100	40	0	27.36	15.53				
case3_7	30.88	27.24	100	40	7	10.88	7.24	0.425	11.621	16.214	35.984
case3_8	28.53	26.06	100	40	8	8.53	6.06	0.425	11.623	16.229	28.421
case3_9	26.17	24.87	100	40	9	6.17	4.87	0.425	11.622	16.219	21.641
case3_10	23.82	23.69	100	40	10	3.82	3.69	0.425	11.622	16.222	15.565
								Prediction after Compensation	10.057	0.568	

Figure 11. Case 3 – Immediate Neighbor Heat Sources [1]

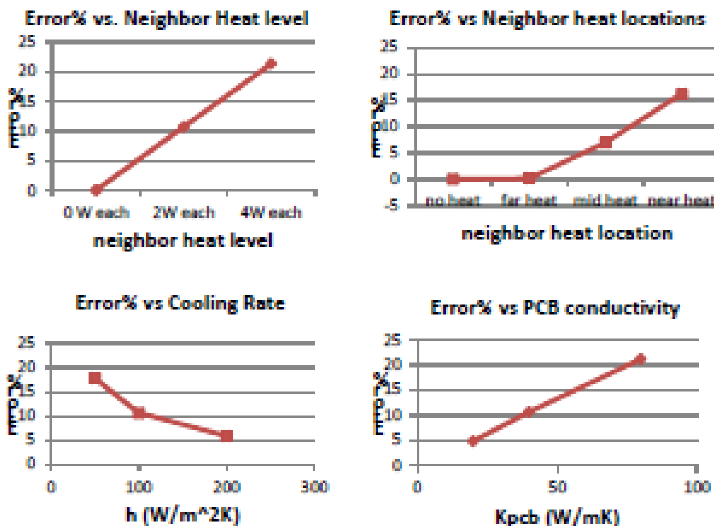


Figure 12. Error (before compensation) Sensitivity [1]

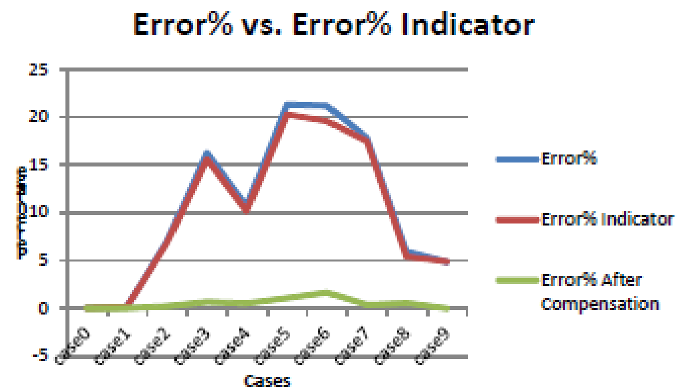


Figure 13. Error % Indicator Effectiveness [1]

As indicated by Equation (7), the model error before compensation is affected by nearby heat sources and their distances to DUT, PCB conductivity, and ambient cooling rate. The errors before compensation are plotted in Figure 12 from case simulation results.

SUMMARY

This new method of measuring the heat flux from a component on PCB under operating condition is innovative and practical way to estimate component heat loss with reasonable error. Comparing this method with traditional calorimetric method, it takes less effort to setup tests by allowing heat spreading through PCB and modulating heat from the case top.

REFERENCES

1. Zhongwei, Qi. , "A Method to Measure Heat Dissipation from Component on PCB", General Electric Technology Infrastructure Healthcare

2. Sajith, V., Balakrishna, C., Sobhan, P., "Characterization of Heat Dissipation from a Microprocessor Chip Using Digital Interferometry

3. Zhang, Y., Janhs, T., "Power Electronics Loss Measurement Using New Heat Flux Sensor Based on Thermoelectric Device With Active Control"