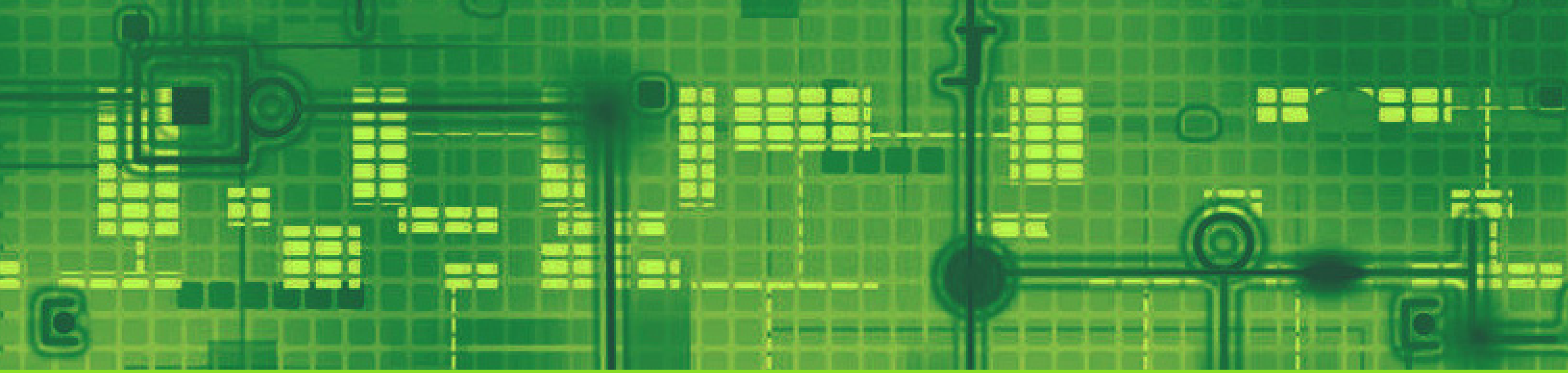

Boundary Condition Dependency

of Junction to Case Thermal Resistance

Introduction

The junction to case (θ_{jc}) thermal resistance of a semiconductor package is a useful and frequently utilized metric in thermal management of electronics. This metric is not an intrinsic property of the device but depends to some extend on the cooling condition at the case surface intended for heat sinking. Also, θ_{jc} can be measured only with limited accuracy by the methods existing today.

This article investigates the dependence of the θ_{jc} of power packages on different cooling boundary conditions and gives an assessment of the accuracy of two measurements methods: the traditional method using thermocouples to measure the case temperature and the recently proposed transient dual interface (TDI) method. This accuracy is measured against results generated by computer simulations.

Background

The Joint Electronic Device Engineering Council (JEDEC) standard JESD51-1 [1] defines the junction to case thermal resistance as follows: the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface. The conventional and still quasi-standard measurement procedure (referred to herein as "thermocouple measurement") requires the measurement of the junction temperature T_J, of the case temperature T_C, and of the power dissipation P, while the device (according to above definition) "is properly heat-sunk", for instance in contact with a water-cooled heat sink. The junction-to-case thermal resistance θ_{jc} is then calculated using:

$$\theta_{jc} = \frac{T_j - T_c}{P} \qquad (1)$$

Figure 1 presents a test set up for measuring θ_{jc} [2]. JEDEC standards requires that all device surfaces, except the top surface (case), be properly insulated. This requirement includes the PCB on which the device is mounted. This way the vast majority of heat dissipated by the electronic device is transferred through the case surface. The cold plate usually attached to the case surface has the role of maintaining the surface isothermal thus reducing any potential measurement error.

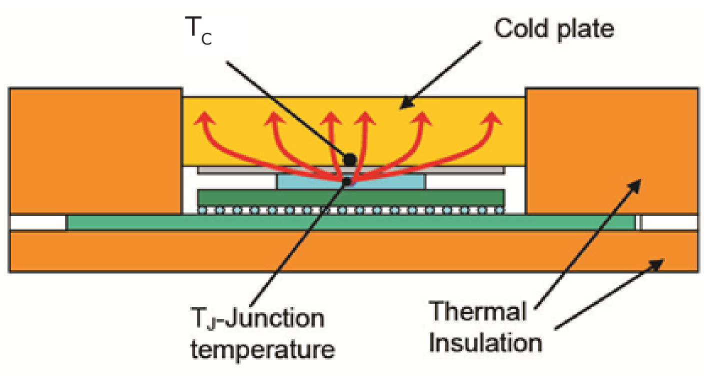

Figure 1. JEDEC Test Setup to Determine θ_{jc} [2]

However, this procedure often produces wrong results since the necessary thermocouple measurement of the case temperature is susceptible to errors. It is very difficult to ensure that the thermocouple actually measures the case temperature T_C of the package and not the temperature of the cold plate or some average value in between. Also, different set-ups are likely to produce deviant θ_{jc} values. Therefore transient measurement methods which do not require the determination of the case temperature have been proposed. These methods, although more accurate than those involving thermocouples, have other limiting factors, such as noise in thermal impedance measurement or thermal interface influence.

Computer Simulation

One way of accurately replicating the JEDEC definition of junction to case thermal resistance is through computer simulations. In this case a constant temperature condition at the package case can be easily applied, so the case temperature T_C is truly constant. For this purpose a simplified finite element model of a power semiconductor have been built, with the geometry and material data included in Table 1.

Part	Size/Thickness	Material	Thermal Conductivity (W/m·K)
Cold plate	20 x 20 x 1 mm	Copper alloy	350
TIM	50 µm	Thermal grease	1.2
Leadframe	8 x 8 x 1.25 mm	Copper alloy	350
Die attach	50 µm	Solder	50
Chip	3 x 3 x 0.3 mm	Silicon	148

Table 1. Parameters for Simulation Model

Figure 2 shows simulation results obtained for two different boundary conditions. A constant case temperature boundary condition and a power dissipation of P = 5W yields 3.12°C maximum temperature difference between junction and case, so the θ_{jc} is θ_{jc},fixed = 0.62 K/W (Figure 2 a). When a "floating" case temperature boundary condition is applied (for this case the temperature of the bottom side of the cold-plate instead of the case temperature is kept constant) the temperature difference between junction and case is 2.66°C and therefore θ_{jc},float = 0.53 K/W (Figure 2 b), a value about 15% lower than the one obtained with constant case temperature BC.

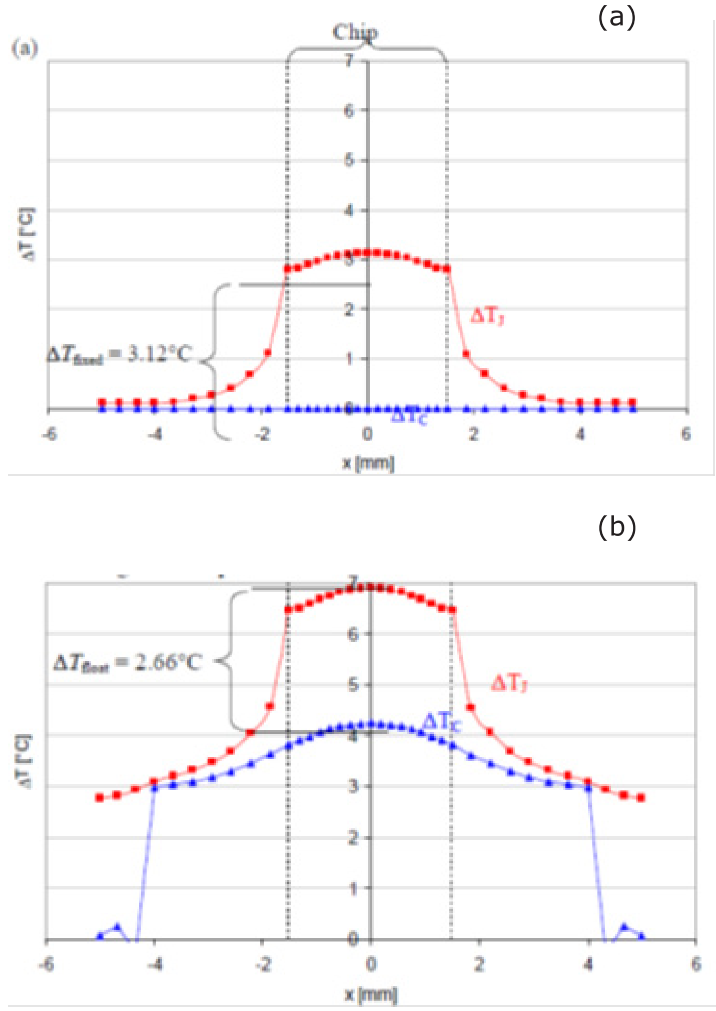

Figure 2. Temperature Distribution on Chip and Case Surface, (a) Constant Case Temperature Boundary Condition, (b) Floating Case Temperature Boundary Condition [3]

The explanation for this result may reside in the different heat flux distributions established as a result of the two boundary conditions. Figure 3 shows the simulated heat fluxes p (z) (W/mm^2) along the vertical axis (z) through the center of the chip.

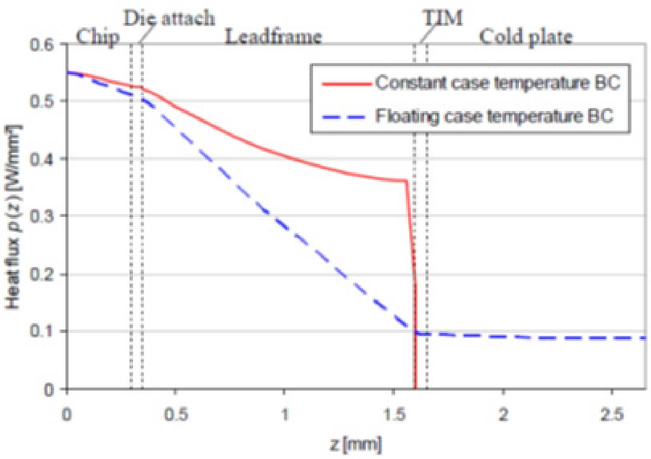

Figure 3. Heat Flux along the z-Axis through the Center of the Chip [3]

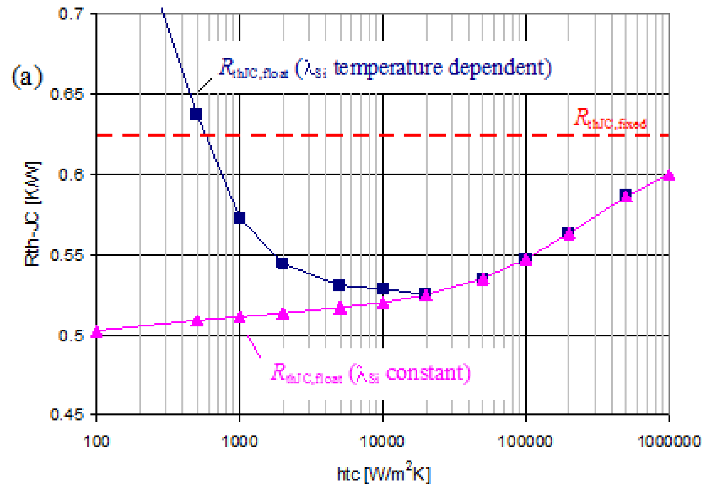

Figure 4. Plot of θ_{jc} versus Heat Transfer Coefficient [3]

θ_{jc} as a Function of the Heat Transfer Coefficient at the Case Surface

The computer model was utilized further in order to study the influence of the cooling condition at package case on the θ_{jc}. A constant heat transfer coefficient h in the range from 100 W/m²K to 106 W/m²K was applied at the case surface of the package model. The results of the simulations are shown in Figure 4. For constant silicon thermal conductivity, the θ_{jc} increases monotonically as expected with increasing heat transfer coefficient and is largest for the constant temperature boundary condition (h =∞). If the temperature dependence of silicon thermal conductivity is taken into account, the θ_{jc} increases also at the low end of the h range.

The maximum difference between the floating and the fixed case temperature θ_{jc} falls in the operating range of liquid cooled cold-plates which are normally used for θ_{jc} measurements. In this case the maximum difference is 0.1 °C/W, i.e. $\theta_{jc,fixed}$ is 19% higher than $\theta_{jc,float}$. For devices with a lower θ_{jc} this deviation can even be larger than 30% as will be shown below.

It should also be mentioned that the chip power dissipation has a small influence on θjc, since the chip temperature and therefore the thermal resistance of the chip depends on it.

Comparison with Measurements

The junction to case thermal resistance for a typical MOSFET device has been determined by three methods: computer simulations, steady state (thermocouple) measurements as well as transient measurements. The thermocouple measurements were done in two different thermal laboratories using different set-ups (apparatus I and II). As a general observation, the measured values are between 15 % and 58 % higher than those obtained from simulations with constant case temperature as a boundary condition (Table 2).

Method	θ_{jc} (K/W)
Simulation with constant temperature boundary condition	0.304
Simulation with floating case temperature boundary condition	0.262
1st Thermocouple measurement with apparatus I	0.35
2nd Thermocouple measurement with apparatus I	0.38
1st Thermocouple measurement with apparatus II	0.42
2nd Thermocouple measurement with apparatus II	0.48
1st Transient dual interface measurement	0.28
2nd Transient dual interface measurement	0.29
3rd Transient dual interface measurement	0.26
4th Transient dual interface measurement	0.29
5th Transient dual interface measurement	0.29

Table 2. Comparison of θ_{jc} Obtained with Different Methods

The third group of θ_{jc} values in Table 2 is the result of transient dual interface (TDI) measurements. This method requires two thermal impedance measurements of the same power semiconductor device in contact with a cold plate. Each of these two measurements is performed with a different interface layer between package and cold plate, causing the two thermal impedance curves to separate. The separation point of the curves and/or the separation point of the corresponding structure functions can be evaluated to obtain the θ_{jc}. The advantage of this method is that the measurement of the case temperature is not necessary any more, thus avoiding all problems related to the thermocouple measurement. However, the accuracy of the TDI measurement is limited by other factors, e.g. by noise in the thermal impedance measurement, the influence of the thermal interface on the separation point, and the limited resolution of the structure function [4]. Based on the experience of several hundred measurements and on comparisons with simulations it is estimated that the accuracy of the TDI method is about 15% (as indicated by the error bars in Figure 5), significantly better than the thermocouple measurements.

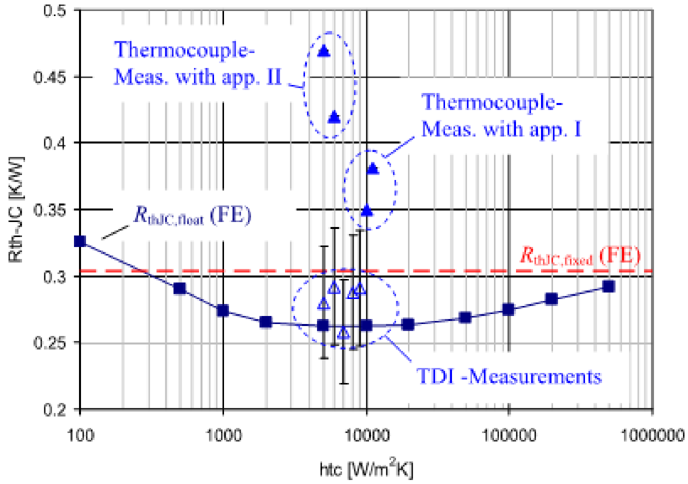

Figure 5. Comparison of the θ_{jc}: Simulated and Measured Values [3]

Conclusions

The junction to case thermal resistance (θ_{jc}) of a semiconductor package is not uniquely defined, but depends on the cooling condition at the package boundary (case). Computer simulations predict differences up to 31% between θ_{jc} values computed with constant and with floating case temperature boundary conditions.

Measured values of θ_{jc} are 15 % to 58 % higher than those predicted by the corresponding simulation with constant case temperature boundary condition. This is a consequence of the fact that thermocouple measurements almost always overestimate the θ_{jc}. It is very difficult to ensure that the thermocouple actually measures the case temperature TC of the package and not the temperature of the cold plate or some average value between the two. Also, different set-ups are likely to produce deviant θ_{jc} values. Transient dual interface measurements, which are accurate to about 15%, are so far the only known way to produce more reliable measurement results.

The boundary conditions must always be stated to enable a fair comparison between the θ_{jc} values obtained through different methods. In order to have a realistic common base for simulated and measured values, a heat transfer coefficient boundary condition (in the operating range of a liquid-cooled cold plate) should be defined and applied in all simulations.

While there is a considerable difference between the θ_{jc} values for constant and floating case temperature boundary conditions, this difference is of little practical importance, since θ_{jc} constitutes usually only a small part of the total junction-to-ambient thermal resistance.

References:

1. **Electronic Industries Association, Integrated Circuit Thermal Measurement Method – Electrical Test Method, EIA/JEDEC Standard, JESD51-1, 1995 [www.jedec.org].**
2. **Advanced Thermal Solutions, Inc., Qpedia magazine,"JEDEC-Driven Resistances", Volume II, 2008.**
3. **Schweitzer, D., "The Junction-To-Case Thermal Resistance: A Boundary Condition Dependent Metric", 26th IEEE SEMI-THERM Symposium, 2010.**
4. **Schweitzer, D., Pape, H., and Chen, L., "Transient Measurement of the Junction-to-Case Thermal Resistance Using Structure Functions: Chances and Limits", 24th IEEE SEMI-THERM Symposium, 2008.**