Conduction-Convection Cooling Solution

for 3D Stacked Electronics

Introduction

Future electronics must provide enhanced functionality within a minimal form factor. To address this demand, 3D stacking of ICs has emerged as an extremely promising technology able to address the performance requirements of tomorrow's high speed computing. This novel technology enables integration of logic, memory, RF and optoelectronic devices on a single chip. The miniaturization comes with the penalty of significant thermal management issues, however. The rate of heat generated per unit volume and thermal resistance increase significantly with each added layer. Also, heat removal from the chips placed in the middle of the stack constitutes a major challenge.
This article reviews the design and thermal parametric study of a unique liquid interface thermal management solution for a 3D chip stack.

Concept Description

Several techniques of cooling 3D chips have been proposed [1]. The novel approach presented in this article proposes a sealed cavity embedded within a heat sink base. The cavity is filled with a dielectric liquid (FC 77) and contains the 3D stack. Internal copper spreader layers are integrated with the 3D stack. The resulting pyramid-like structure allows for lateral heat transfer from the stacked devices and promotes natural convection (Figure 1). The pyramid is submerged in a dielectric liquid so that heat is transferred from the external surfaces of the lateral spreaders to the liquid by natural convection. Ultimately, heat from the liquid is transferred to a radial heat sink mounted on the heat sink base as illustrated in Figure 2. An important aspect of the integration of the 3D chip stack to the radial heat sink is the thermal interface between the stack and the heat spreader. The present direct liquid immersion interface significantly reduces thermal resistance, allows for extremely compact packaging, alleviates thermo-mechanical stresses, and is easily scalable.

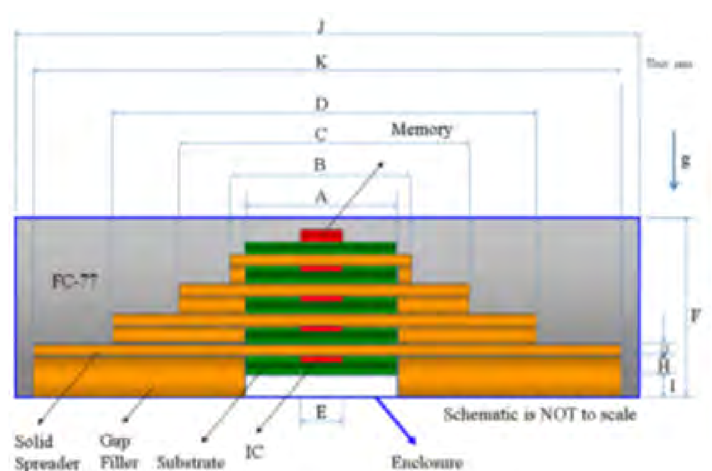

Figure 1. Immersion Cooling of 3D Stack [2]

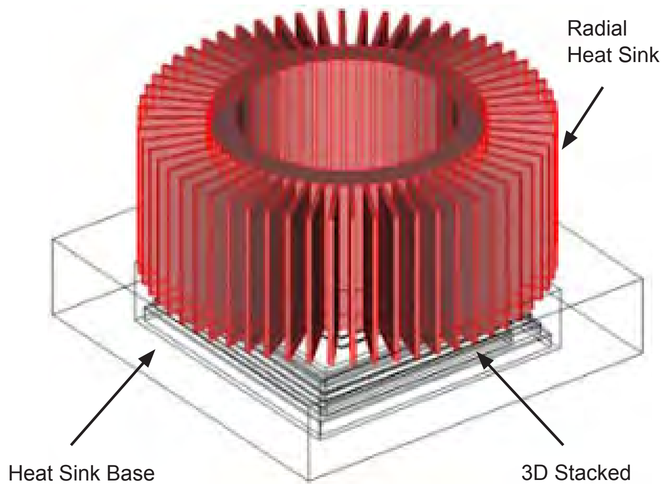

Figure 2. 3D Stack Embedded in an Enclosure in the Heat Sink Base [2]

Numerical Model

For the baseline simulation, an ambient temperature of 298 K and a heat load of 10 W for each IC and 1 W for the memory chip on the top of the stack were assumed. Figure 3 shows a heat sink assembly as well as the flow between the fins of the radial heat sink. Synthetic jets are formed by time-periodic alternating suction and blowing of fluid through a small orifice, generated by an electromagnetic driver confined in a cavity.

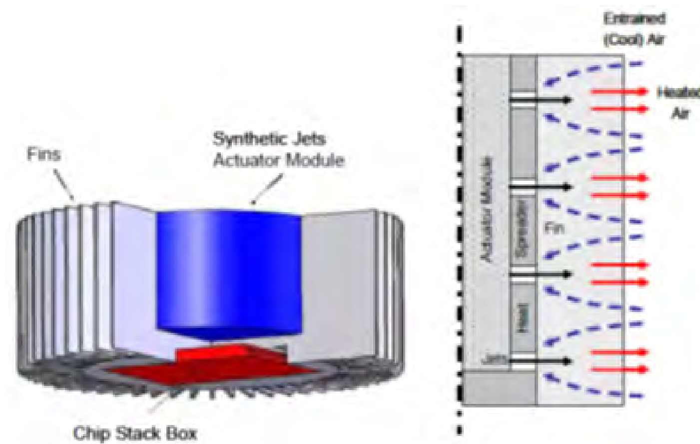

Figure 3. Heat Sink Assembly (Left) and Jet Induced Flow (Right) [2]

These jets have been demonstrated to provide heat transfer coefficients around 50-80 $W/m^2 \cdot K$. For the simulations, a heat transfer coefficient of 70 $W/m^2 \cdot K$ was assumed. The radial heat sink has 60 fins distributed radially. The fins are 0.9 mm thick and 12.7 mm long. Also, the heat sink incorporates a 5 mm thick vertical heat spreader.

Table 1 lists the material and thermophysical data used in the simulations. The properties of the dielectric fluid were considered as temperature dependent.

Part	Material	Thermal Conductivity (W/m·K)	Density (kg/m^3)	Specific Heat (J/kg·K)	Dynamic Viscosity (Pa·s)
Substrate	FR4	0.3	1900	1369	
IC	Si	163	2330	703	
Heat Spreader	Cu	400	8700	385	
Dielectric Fluid	FC-77	$0.065-8 \cdot 10^{-5}T$	1838-2.45T	1014+1.554T	$56.25 \cdot 10^{-5}$
Dielectric Fluid	Cu	400	8700	385	
Heat Sink Base	Cu	400	8700	385	
Heat Sink	Cu	400	8700	385	
Solder Bumps	Pb-Sn	50			
TIM	Product	9			

*T is the temperature in ºC

Table 1. Material and Thermophysical Property Data

Results

The model was used to solve the conjugate conduction-convection problem for the entire simulation domain (from chip to ambient). Figure 4 shows the temperature distribution, with the maximum temperature being 341.75 K. The temperatures of the four ICs in the stack for the baseline power distribution mode (QA) are included in Table 2. For all the simulations, the spreaders and the ICs were numbered from 1 to 4 starting from the bottommost tier.

Mode of IC Power Distribution	Power Dissipation (W)				Temperature (K)			
	IC1	IC2	IC3	IC4	IC1	IC2	IC3	IC4
QA	10	10	10	10	340.04	340.04	339.83	337.8

Table 2. IC Temperatures

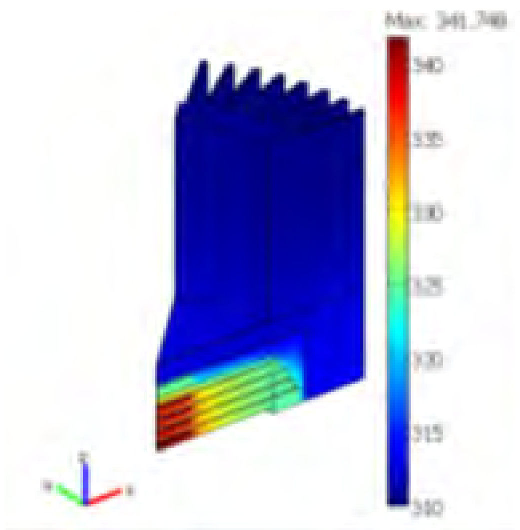

Figure 4. Temperatures (K) for the Heat Sink with Integrated 3D Stack [2]

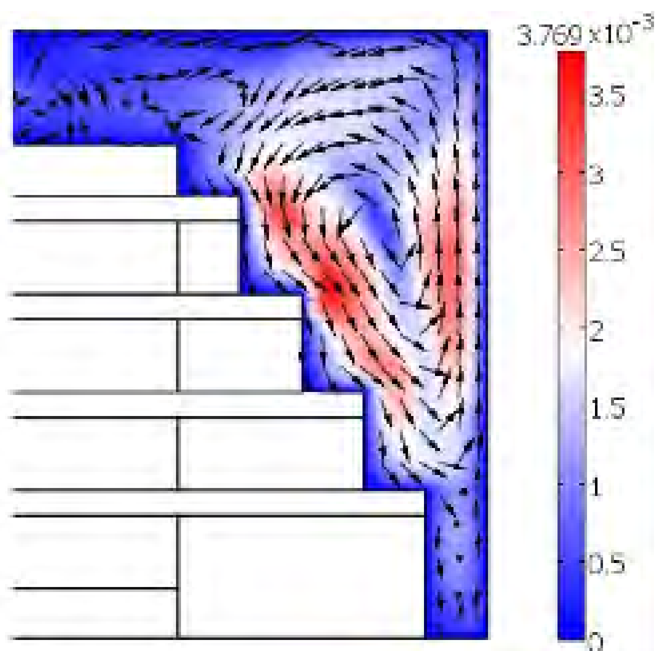

Figure 5. The 3D Velocity Field (m/s) in the Dielectric Liquid [2]

Figure 5 shows the induced natural convection velocity field between the edges of the stack and the enclosure surfaces. Despite the fact that the height of the stack enclosure is only a few millimeters, strong natural convection of the FC-77 is present over the entire fluid domain. This effect is likely due to the truncated pyramidal arrangement and will not be possible if no spreaders are used, or by using same size spreaders.

Parametric Study

The results of the baseline simulation show that two thermal resistances are the dominant ones in the resistance network: the liquid interface thermal resistance and the fin to air thermal resistance. Since synthetic jets were analyzed in detail in prior work [3], key parameters affecting the thermal resistance of the liquid interface were varied and their effect on natural convection mechanism within the enclosure studied.

Effect of IC Power Distribution

It is possible that the ICs in a 3D stack will not dissipate the same power. Therefore, in addition to the base heat load distribution (QA) described before, two other power configurations were assumed. Table 3 shows the power distribution modes and the volume averaged temperatures in the ICs corresponding for these modes.

Mode of IC Power Distribution	Power Dissipation (W)				Temperature (K)			
	IC1	IC2	IC3	IC4	IC1	IC2	IC3	IC4
QA	10	10	10	10	340.04	340.04	339.83	337.8
QB	15	10	10	5	345.39	340.66	339.75	333.22
QC	5	10	10	15	326.75	330.82	331.10	333.31

Table 3. Effect of Power Distribution Modes on IC Temperatures

As expected, it was found to be advantageous to place the highest power distribution IC on the largest spreader and locate it close to the radial heat sink base.

Effect of Solid Spreader Length

Copper spreaders of various dimensions were explored with a goal of minimizing the footprint of the 3D stack. Table 4 shows the volume averaged temperatures in the ICs for different lengths of the bottommost spreader L1.

Spreader Length L1 (m)	Temperature (K)			
	IC1	IC2	IC3	IC4
42.5	372.49	369.84	362.15	347.77
52.5	340.04	340.04	339.82	337.80
60	331.84	331.86	331.73	347.77

Table 4. Effect of Spreader Length on IC Temperatures

It appears that there is an optimal spreader length (L1 = 52.5 mm) that maintains stack temperatures uniform, an important aspect for thermal stress mitigation.

Effect of Solid Spreader Thickness

Since conduction through solid spreaders plays a crucial role in the proposed cooling concept, the spreader thickness was varied for the next step of the parametric study. Table 5 includes the volume averaged temperatures in the ICs for spreaders with uniform thickness. As observed before, the temperature distribution across the ICs is relatively uniform.

Spreader Thickness t (μm)	Temperature (K)			
	IC1	IC2	IC3	IC4
250	348.90	348.83	348.15	343.85
500	340.04	340.04	339.82	337.80
750	331.84	331.64	331.50	347.17

Table 5. Effect of Spreader Thickness on IC Temperatures

Conclusions

This article presents a novel concept for a single phase liquid interface that can result in effective heat transfer from a high power, high density 3D IC stack. The concept was proven via numerical simulations. The enclosure containing the 3D stack is then integrated into the base of a radial heat sink. The heat sink fins are cooled by synthetic jets with a heat transfer coefficient of ~70 W/m^2K. The suggested design is suitable for compact applications and is an ideal candidate for scaling.

It was observed that enhancing natural convection in narrow horizontal enclosures is viable and effective. The effectiveness of this concept depends on proper design of the key components and apt choice of parameters like the spreader length and thickness. It was shown that intelligent placement of the solid spreaders (depending on the heat load distribution and thermal conduction resistance in the solid spreader relative to the convection resistance in the fluid) play a crucial role in minimizing the 3D stack thermal resistance.

Although promising, the concept needs experimental validation as well. Also, since it involves liquids, issues associated with liquid containment and handling are to be expected and have to be addressed.

References:

1. **Advanced Thermal Solutions, Inc., Qpedia magazine," Cooling Solutions for 3D Stacked Chips", Volume III, 2013.**

2. **Kota, K., Hidalgo, P., Joshi, Y. and Glezer, A. "A Novel Conduction-Convection based Cooling Solution for 3D Stacked Electronics", 26th IEEE SEMI-THERM Symposium, 2010.**

3. **Gerty, D., Gerlach, D., Joshi, Y. and Glezer, A. "Development of a Prototype Thermal Management Solution for a 3-D Stacked Chip Electronics by Intervealed Solid Spreaders and Synthetic Jets", THERMINIC 2007.**

108K+

heat sink configurations

ATS ADVANCED THERMAL SOLUTIONS, INC.

Innovations in Thermal Management®

www.qats.com

pushPIN™

The **largest** selection of push pin heat sinks available on the market