

# New Design Concepts in 3D Stacked

## Chips and Their Thermal Challenges

In today's mobile handset market the trend is to provide high performance, low cost components with integration of functionality and small form factor. The ever increasing demand of handset makers to provide smaller, thinner and lower cost packaging solution drives the packaging industry to develop packages that integrates more devices in the same footprint in which devices are integrated within the package in vertical direction, named 3D packaging. In this, the logic device and memory devices are packaged and tested together and then stacked together in a package form typically known as package on packages (POP) technology which is popular and widely used in mobile phone industry.

The POP approach is limited by the fact that the connection between packages is made with solder balls at the periphery of top package to the top of bottom package making the package thicker and taller than an equivalent stack. The POP can be made thinner by reducing the substrate thickness but it leads to package warpage problems. The new generation of stacked packages called fan in package on package (FiPOP) addresses the limitation posed by POP of increased size and thickness. In FiPOP package, the connection between top and bottom packages is made by means of a Center ball array instead of peripheral ball array. This allows reduction in top package size [1]. The connection to the bottom package is provided by means of wire bonds which allow the bottom package to be smaller. The FiPOP allows the

use of thinner substrate to reduce height without warpage.

### FiPOP Structure

The exposed interconnect land array on top centre surface of bottom package in FiPOP which is different than conventional POP package having interconnect land array at the top periphery allows the top interconnect array to "fanned-in" towards the centre of the bottom package, thus named as "fanned-in" POP to differentiate with conventional POP typically called "fanned-out" interconnect array.

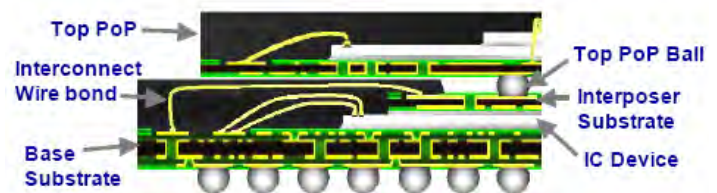


Figure 1. FiPOP Internal Structure [1]

Figure 1 is the detailed view of FiPOP structure and shows interposer substrate connected to the bottom package to allow interconnect to the top package. The interposer substrate is a thin laminated packaging substrate which is mounted on the top of the bottom package using similar manufacturing process and material used in conventional packaging. This interposer is electrically connected to the base package using wire bonds at the

periphery. The terminal from the top package is routed to the edge of the interposer, connected to the base substrate by wire bonds and then routed to interconnect with the device mounted to the base substrate and routed to a terminal on the bottom of the package. The wire bond interconnect helps to reduce the package size as the wire bond interconnect at the periphery is much denser than the solder ball interconnect used for conventional POP. Decreasing the package size in FiPOP makes it competitive as compared to conventional POP.

The top central land pattern used in FiPOP allows using more conventional centre ball grid array package on top. In conventional POP, top package needs to be of the same size or larger than the bottom package to enable the peripheral ball interconnect. The FiPOP allows decoupling bottom package size with top package thereby use of smaller top memory package is possible [1]. Even an “off the shelf” top package such as FBGA can be mounted on the top of the FiPOP but use of such standard packages does not satisfy the minimum size and thickness requirement as desired by mobile electronic industry and customized thin top FBGA’s with minimized size, height are developed to suit the industry requirement.

The FiPOP offers smaller top and bottom package size which is the key consideration for package required in mobile phone applications. The stacked POP is the thickest package which is not suitable to current and future phone industry requirement where minimum size and thickness is critical. Even though the FiPOP package has interposer substrate added on the top of the bottom package, the equivalent or lower stack up height as compared to conventional POP can be achieved by using a thinner base substrate and by minimizing the top to bottom package gap [1]. Figure 2 shows comparison of typical POP and FiPOP stack up height.

This achievement is possible due to better co-planarity, flatness and having less warpage during reflow process. For conventional POP package to achieve the acceptable flatness requires thicker base substrate. This is because the periphery of the POP is not covered by encapsulant mold compound (EMC) and therefore more susceptible for warpage during reflow process. In FiPOP, the EMC extends to the edge of the package allowing thinner base substrate without excessive warpage. Flatness control of the FiPOP is the key factor for reducing the stacked height.

Item	POP	FiPOP
All Die Thick	0.075 mm	0.075 mm
A	0.18 mm	0.20 mm
B	0.30 mm	0.24 mm
C	NA	0.26 mm
D	0.39 mm (0.48 mm ball)	0.12mm (0.25 mm ball)
E	0.51 mm	0.51 mm
<b>Total PKG Thickness</b>	<b>1.38 mm</b>	<b>1.33 mm</b>

• A : Bottom solder ball height      • D : Ball height for top PKG mounting  
 • B : Bottom substrate thickness    • E : Top PKG (substrate + Mold cap) thickness  
 • C : Bottom mold cap thickness

### Thermal Design Considerations

With reduced package size and improved package performance, thermal management of 3D stack package poses great challenge to thermal engineers even with moderate power consumptions. Because of size and cost constraint, external cooling solutions such as heat sink and fan are not recommended for mobile phone thermal management and it is a challenge for this industry and package manufacturers to find a way to dissipate the heat effectively without external cooling methods.

Providing a thermal path for heat dissipation is the only option to maintain the junction temperature that meets the thermal requirements of the

Figure 2. FiPOP and POP Stack Up Height Comparison [1]

device. In a typical package construction there are two ways to dissipate the heat from junction to ambient. One is through conduction from die via substrate and then from solder balls to PCB. The heat from PCB is dissipated to ambient via convection/Radiation. The second mode is conduction from silicon die via mold compound to the top of the package and then heat is dissipated to ambient via convection/radiation from this surface. Previous studies suggest that because of small surface area, very little heat is transferred to ambient from the package top surface.

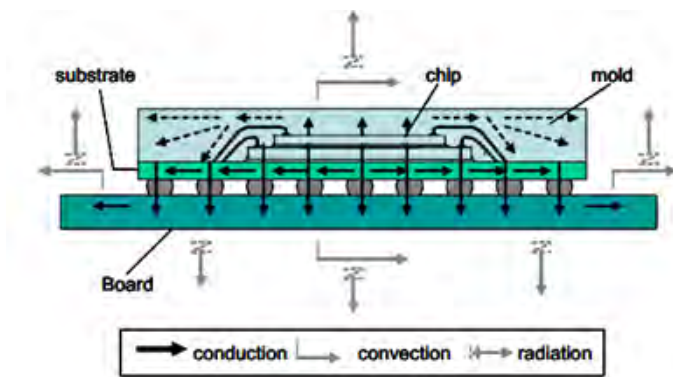


Figure 3. Heat Flow Path From Die to Ambient [2]

Figure 3 shows heat dissipation paths in a typical stacked package. The dotted lines are the less efficient thermal paths from die to molding compound to ambient [2]. The solid lines shows efficient heat flow path from die to ambient through the substrate, solder balls and the PCB routing.

For stacked packages there are many factors affecting the thermal performance, but the primary factors can be grouped into three main categories: geometry, material and environment. The stack up geometry and material are related to the package internal thermal design while the environmental category is related to factors outside the package such as handset size, PCB design, parts, etc. In early design studies of packaging, it will be difficult to predict system-level design impact due to wide variety of customer handset designs. In the material category itself the selections are restricted primarily by moisture sensitivity requirements and cost,

resulting in a limited choice for material selection impacting thermal performance.

### Effect of Package Parameters on FiPOP Thermal Performance

Cher Bai et al. [2] studied the effect of package parameter on thermal performance of Chip Scale Package (CSP) and the study suggests the die size and solder ball I/O pattern have the most impact on package thermal performance.

Nagedrappa et al. [3] further implemented the findings from [2] to thermally investigate in detail the impact of package parameter on performance of FiPOP and studied the effect of three variables: die size, solder ball I/O pattern and number of thermal vias. The following highlights the results of finding by Nagedrappa et al.

### Number of Thermal Vias

In FiPOP, Vias are used for routing of signals from bond finger to solder balls through substrate. Thermal vias can be added to improve conduction. A rectangular via pattern created under die footprint is studied [3]. The effect of via pattern without solder ball is studied for 24, 29, 34, 39, 44 and 49 vias. Each via has 100 micron drill diameter and 10 micron plating thickness. The vias were placed under bottom package only and thermal performance of package was tested for top die loading and bottom die loading.

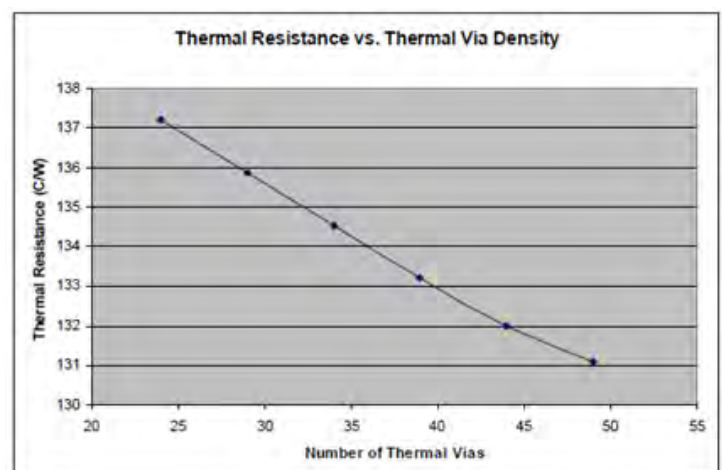


Figure 4. Effect of Thermal Via Density On Thermal Resistance [3]

Figure 4 shows the behavior of thermal performance of the package under varying via numbers. There is a small reduction in thermal performance of FiPOP when thermal vias are added alone [3]. When top die was loaded only, 0.5% improvement was seen with 104% increase in via density. This implies that thermal vias added to the bottom package have little impact on top package thermal performance.

## Solder Ball I/O Density

In FiPOP package configuration solder balls are used for I/O signals. An increase in number of solder balls are expected to improve thermal performance. The detailed study was carried out by adding extra solder balls to the thermal vias under the die foot print. Along with baseline solder ball configuration additional 5, 10, 15, 20 and 25 extra solder balls are added to the thermal vias [3].

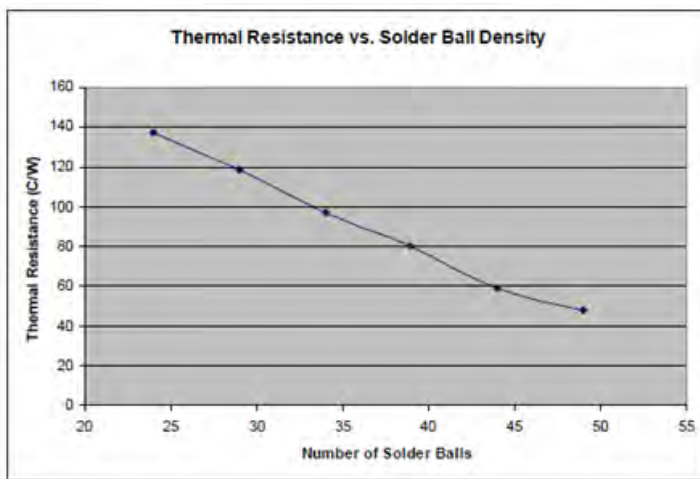


Figure 5. Effect of Solder Ball Density on Thermal Resistance [3]

Figure 5 shows the effect of solder balls on the thermal performance of FiPOP. The addition of solder balls at the bottom package has significantly improved package thermal performance. Also the results indicate that adding thermal vias without solder ball is ineffective and solder ball must be added along with thermal vias to improve the package thermal performance [3].



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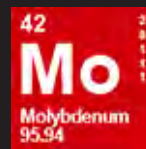
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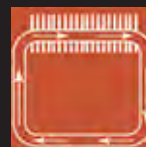
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### Die Size Variation

The effect of die size on thermal performance of FiPOP package was studied for 81, 72.9, 64.8 and 56.7 mm<sup>2</sup> [3]. To understand the impact of die size irrespective of thermal vias or solder ball, no thermal vias or solder balls were added directly under the die area.

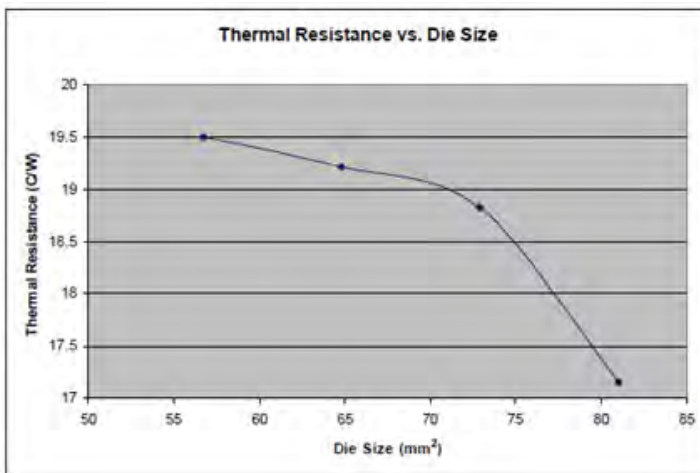


Figure 6. Effect of Solder Ball Density on Thermal Resistance [3]

Figure 6 shows that smaller the die size higher the package thermal resistance and is contributed to higher heat flux and increased spreading resistance. For bottom die loaded cases, 10% increase in die area results in 2.8% improvement in thermal resistance of the package. In top package loading case, 10% increase in die area results in 8.7% improvement in package thermal resistance.

From the previous studies, it is shown that FiPOP package thermal resistance decreases with increase in thermal vias and solder balls [3]. It is also shown that thermal vias alone cannot help improve thermal resistance significantly. However addition of solder ball provides significant improvement in package thermal performance. Consequently the die size has significant impact on thermal performance and package thermal resistance decreases with the increase in die size.

### References:

1. Carson, F., Lee, S, Yoon, S. "The development of the fan-in package-on-package". Paper presented at the 2008 58th Electronic Components and Technology Conference, 956-63.-2008
2. Bai, C., and Veatch, M. "Chip Scale Package Design for Thermal Performance in Mobile Handsets". Paper presented at the 2007 Electronic Components and Technology Conference, 1415-19-2007
3. Nagendrappa, N, Okamoto, O, and Barez, F., "Thermal Characterization of Fan-in Package-on-Packages". paper presented at the 26th IEEE Semiconductor Thermal Measurement & Management Symposium – 2010

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