Thermal Conductivity of

Printed Circuit Boards

When performing an analysis of heat generating electronic components on a printed circuit board (PCB or PWB), the PCB is often used to dissipate a significant portion of the heat. Some components are designed to dissipate heat with the use of a heat sink, and they often have a low resistance from their junction to case (Θ_{jc}) in order to facilitate the thermal transfer. When specifying heat sinks for these components, the heat dissipated through the PCB can still be significant, but it depends on operating conditions and PCB design.

To begin examining these questions, JEDEC provides standards for the purpose of evaluating the junction-to-ambient resistance (Θ_{ja}) of leaded surface mount packages, known under JESD51-3 and JESD51-7. The former dictates the construction of a PCB with "low effective thermal conductivity", and the latter specifies more copper layers for a "high effective thermal conductivity" [1,2]. Of course, in specific applications, the construction of PCBs can vary widely, and Lohan et al. describe a few other configurations that they decided to test and compare to the JEDEC standards [3].

In Figure 1, Configurations 1 and 2 represent the JEDEC standards, with low and high thermal conductivity designs, respectively. Configuration 3 is similar to the JEDEC high thermal conductivity board, but has additional full copper planes and layers with signal traces. In addition to PCBs made from the traditional FR4 fiberglass material, Lohan et al. also tested two PCBs with metal substrates, also known as Metal Core PCBs (MCPCB). These

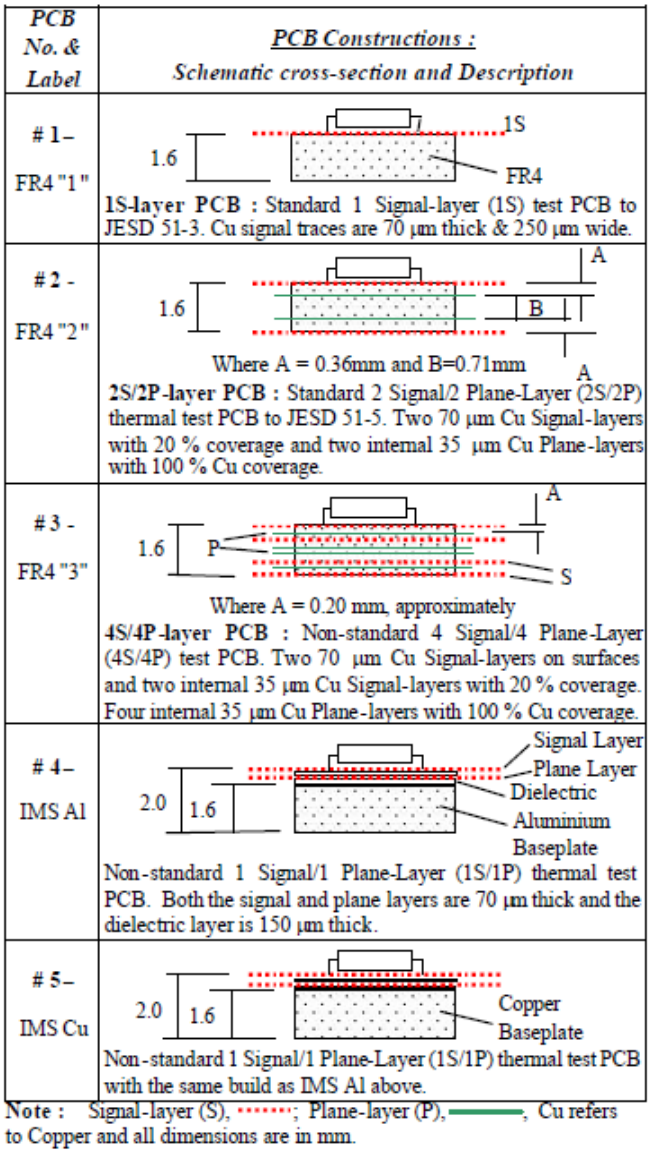

Figure 1. JEDEC Standard and Other PCB Configurations Compared [3]

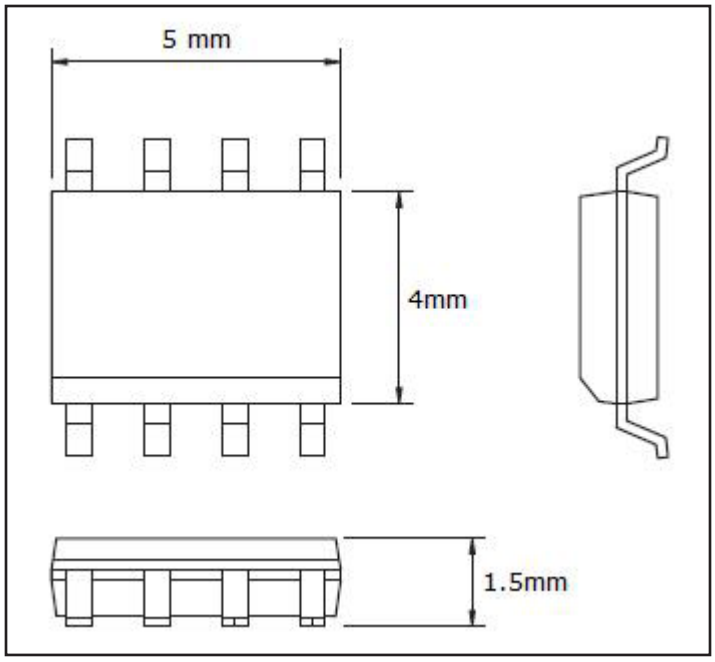

Figure 2. Typical SO-8 Package [4]

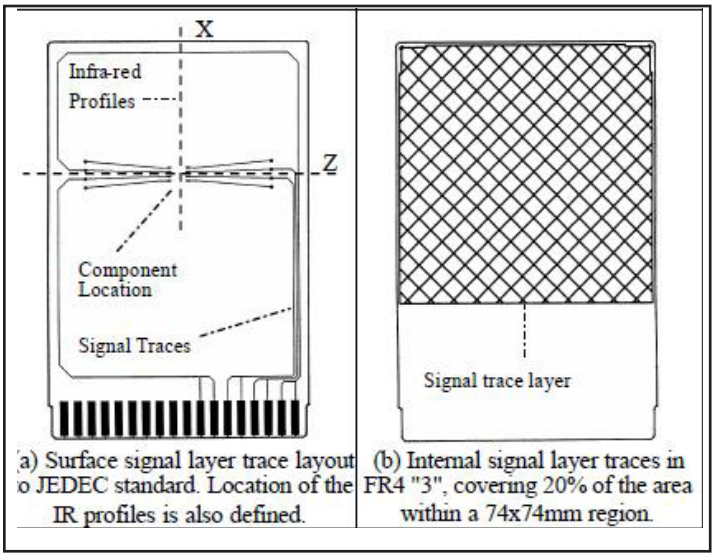

Figure 3. Patterns of Traces on the Test PCBs [3]

cases are shown as configurations 4 and 5, and are most commonly used in LED applications.

These PCB configurations were modeled by CFD simulations, but lab tests were also conducted, using PCB samples with an SO-8 component (Illustrated in Figure 2) as the heat source. The PCB design was defined by the JEDEC standard, shown in Figure 3. This pattern of traces was used for all the different PCB constructions, with pattern "a" used for surface signal layers, and pattern "b" used for internal signal layers. In Figure 1, the "plane layers" are uninterrupted planes of copper. The overall PCB size is 76.2x114mm. [1]

All PCB samples were tested under natural convection conditions defined by JEDEC, which, among other guidelines, states that the test chamber is a sealed cube 305mm in dimension [5]. Two samples were tested for each configuration and the results were averaged. Die temperatures were monitored by a temperature diode on board each component, and surface temperatures were measured using infra-red thermography.
The results are shown in Figure 4. The junction temperature differences between the 5 PCB configurations clearly show the effects of the metal layer patterns on heat dissipation. For instance, at 0.5W of power level, if T_a is assumed to be 25°C, then there is a 40% reduction in temperature rise from PCB#1 to PCB#2 and 3. The most significant difference between these PCB configurations is that PCB#1 has no continuous copper planes. The MCPCBs, PCB#4 and 5, show a reduction of another 20%, which highlights the advantage of heat spreading in the metal base.

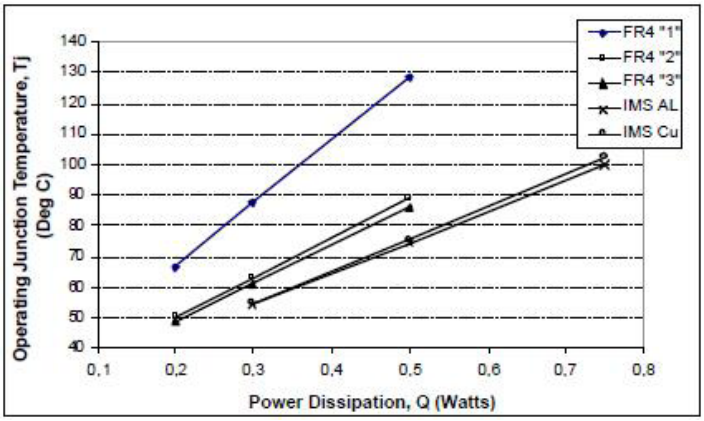

Figure 4. Junction Temperature vs Power Dissipation, as a Function of PCB Type

It is interesting that, in this test, there is not much difference seen between MCPCBs with the aluminum and copper base, even though copper has a thermal conductivity which is twice that of aluminum. This effect is most likely application dependent, because in this scenario, the heat transfer is limited by the convection from the surface of the PCB, and not by the heat spreading within the PCB. In a forced convection application, this could well change. In this test scenario, it appears that there is not much increase in thermal performance as the effective in-plane thermal conductivity ($k_{||}$) rises past 50 W/m-K, as shown in Figure 5 below.

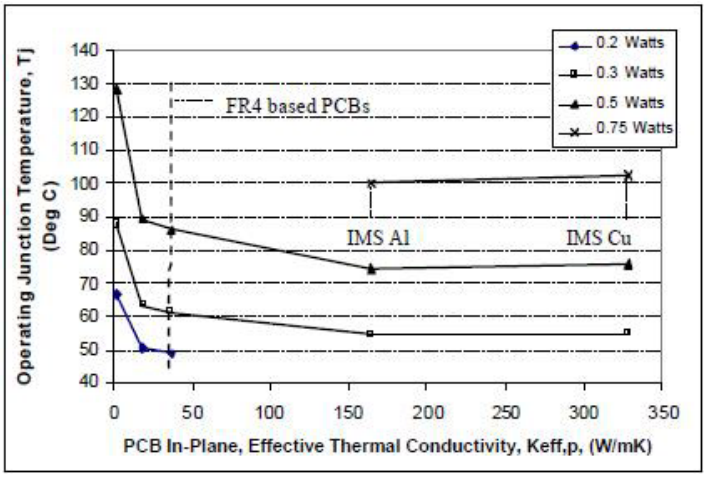

Figure 5. Junction Temperature vs. Effective In-Plane Thermal Conductivity [3]

These results do illustrate the findings by Azar and Graebner, who found that PCB analysis may be simplified by the fact that continuous copper layers dominate the $k_{||}$, and that layers with signal traces can be ignored [6]. Azar and Graebner also found that the thermal conductivity normal to the board ($k_{\perp}$) is determined largely by the k of the substrate. However, in local areas, the presence of many vias can substantially affect the apparent $k_{\perp}$.

Esmailpour [7] documented the effects of vias on PCB thermal conductivity, including the effect of solder-filled vias. In contrast to Lohan et al., who used a simulated component in a natural convection environment, Esmailpour used a test fixture to directly test the effective thermal conductivity of the PCB itself [7]. The fixture includes a heater, the output of which passes through a heat flux column before heating on side or edge of the PCB sample. On the cold side of the PCB, the heat flows through another heat flux column before being removed by a liquid cooled cold plate (See Figure 6 below).

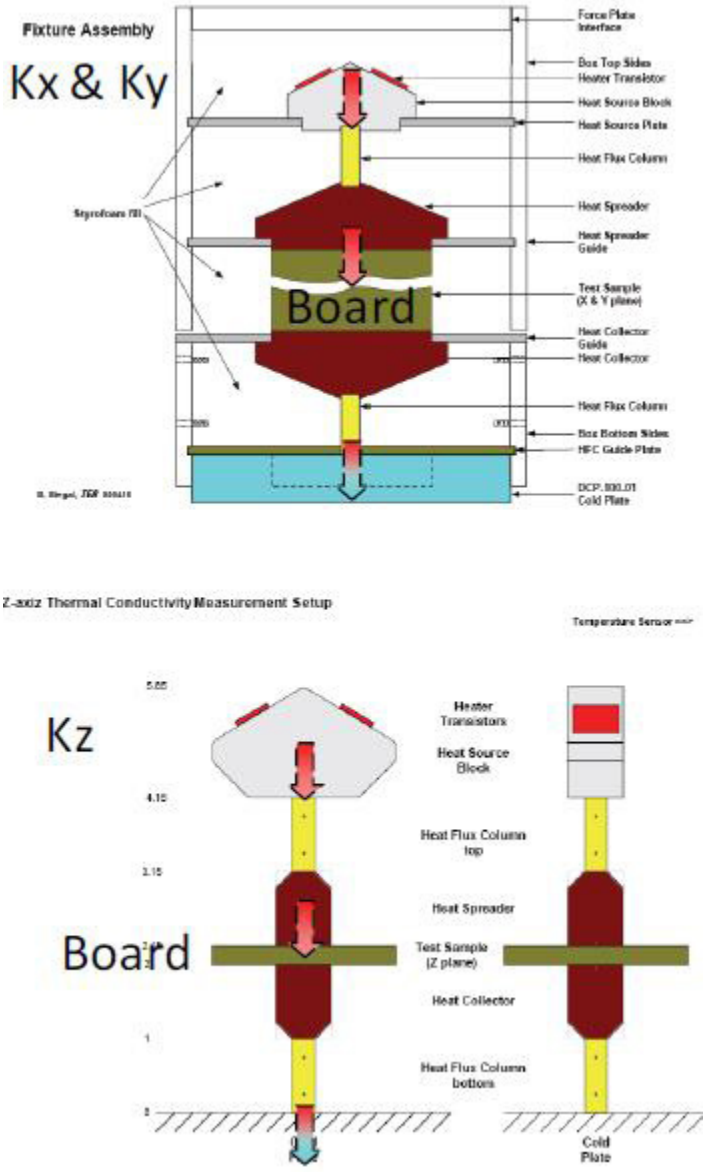

Figure 6. Fixture for Testing Effective $k_{||}$ (top) and $k_{\perp}$ (bottom) of PCBs [7]

Among other tests, Esmailpour compared 3 boards with different land patterns and component type attachments. Each of the boards had the same 24 layer construction with FR4 substrate and different copper layers. The FBGA attachment incorporates vias by default, whereas the DDPAK and PQFP do

not. The PQFP has external leads, and the DDPAK has a heat slug which is normally soldered to a copper pad on the PCB.

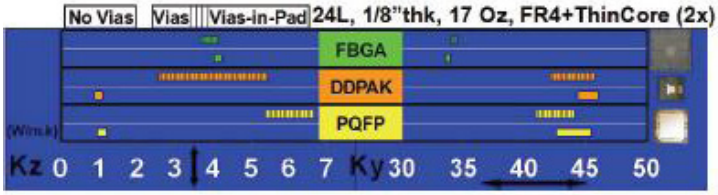

Figure 7. Effect of Vias on Effective Thermal Conductivity in a PCB [7]

The results, shown in Figure 7 above, show a clear increase in $k_{\perp}$ (k_z) with the addition of vias beneath the component (The striped plots indicate the results with vias). In the case of the PQFP, the effective k increased from about 1 W/m-k to 5.5-6.5. It was also observed that the $k_{||}$ (k_y) was reduced slightly by the presence of vias. This is attributed to the vias interrupting the continuity of the copper planes in that area, creating additional resistance to the heat flow. This was also the reason for the lower $k_{||}$ with the FBGA compared to the other two types. As we expect, because the PCB substrate has a dominant effect on the overall $k_{\perp}$, this value is much lower than the $k_{||}$.

Esmailpour also tested the effects of PCB substrates other than FR4, as well as the effect of using solder-filled vias. In a standard FR4 PCB, improvements to $k_{\perp}$ in the neighborhood of 10% could be realized with solder filled vias. The $k_{||}$ improved slightly as well. Copper filled vias or un-filled vias with thicker copper plating are also alternatives, but the price of such PCB construction has to be weighed against the thermal benefit.

The importance of analyzing PCB thermal conductivity has gained new importance with the proliferation of LEDs. These components mount to a PCB as other surface mount components, but because they emit light from the top of their package, it is impossible to place a heat sink on the lens. For this reason, nearly all of the heat generated by an LED passes into the PCB before it is dissipated. In some cases, the PCB is enough to dissipate the heat, but in many others, some sort of heat sink needs to be attached to the back side of the board. Because the PCB plays such a significant part in the thermal management of the LED, its thermal properties must be fully understood. The relationships between the PCB materials and the resulting effective $k_{\perp}$ and $k_{||}$ are fairly straightforward as we have seen. $k_{||}$ may be approximated by looking at just the continuous copper planes (in an FR4 PCB). Because $k_{\perp}$ is dominated by the substrate, MCPCBs can be very effective compared to traditional FR4, but they cost much more. Thermal vias, especially filled vias, may be a more cost-effective alternative, and can potentially improve effective $k_{\perp}$.

References:

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2. **EIA/JESD51-7, "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages", Electronic Industries Association, 1999.**

3. **Lohan, J., Tiilikka, P., Rodgers, P., Fager, C., and Rantala, J., "Effect of PCB Thermal Conductivity on the Operating Temperature of an SO-8 Package in a Natural Convection Environment: Experimental Measurement versus Numerical Prediction", Nokia Research Center, Finland, 1999.**

4. **"Package information – SO8", http://www.diodes.com/_files/zetex_files/pack/SO8.pdf, [December 23, 2013].**

5. **EIA/JESD51-2, "Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still-Air)", Electronic Industries Association, 1995.**

6. **Azar, K., and Graebner, J., "Experimental Determination of Thermal Conductivity of Printed Wiring Boards", Proceedings of the 12th IEEE SEMI-THERM Symposium, 1996.**

7. **Esmailpour, M., "Do You Really Know the Thermal Conductivity of Your Boards?", Teradyne Inc. & UCLA School of Mechanical Engineering, 2009.**